FIGURE 16-A

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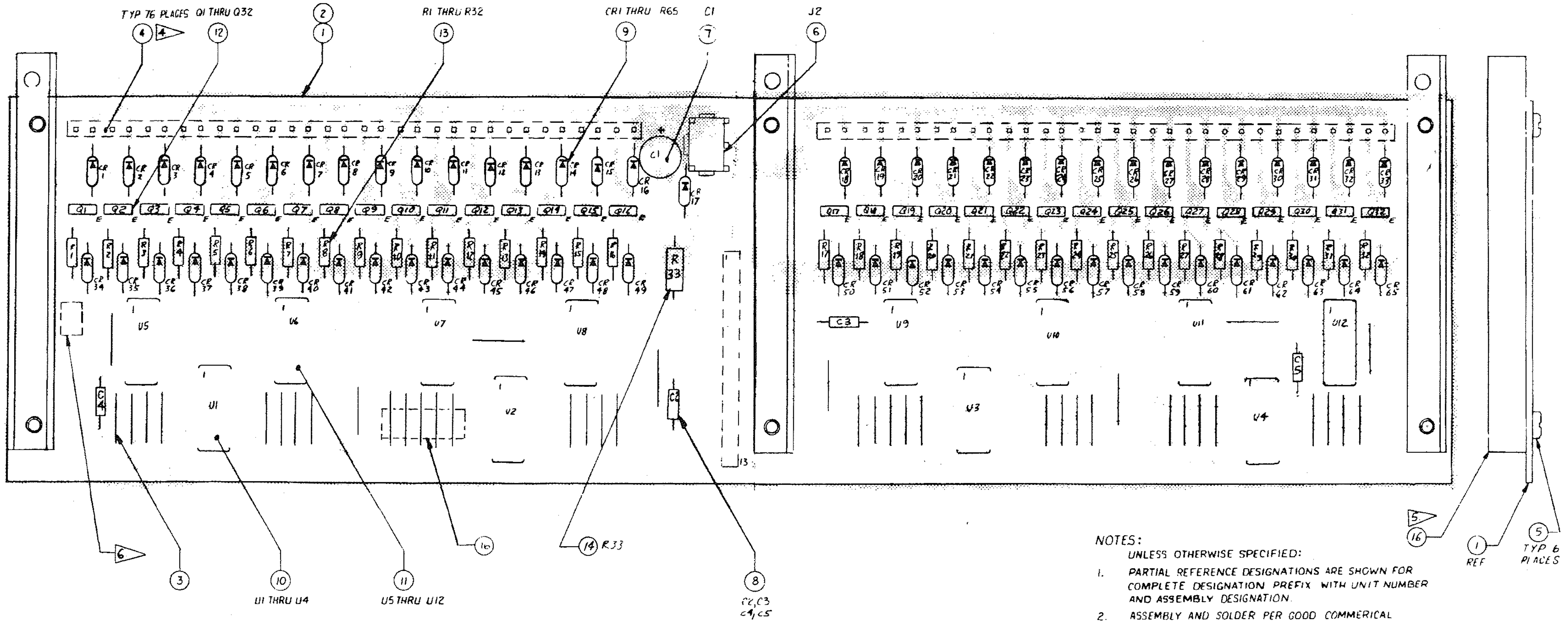
REVISIONS			
A	INC PER ECA 5327	10-11-77	
B	INC PER ECA 5355	10/1/77	
C	INC PER ECA 5384	11/9/77	
D	INC PER ECA 5557		
E	INC PER ECA 5701		
F	INC PER ECA 5875	7-5-78	



NOTES:
UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ASSEMBLY AND SOLDER PER GOOD COMMERICAL STANDARDS.
3. REFERENCE DRAWINGS:
   SCHEMATIC : 100-06E003
   P.W. BOARD : 100-05D003
   P.W. MASTER 100-08D003

4. INSTALL ITEM 4 IN ALL HOLES ENCLOSED INSIDE DASHED LINES

5. FOR A (-1) ASSY SEE PL100-04D003-1
FOR A (-3) ASSY SEE PL100-04D003-3
FOR A (-5) ASSY SEE PL100-04D00[illegible] 5

6. RUBBER STAMP REVISION LEVEL, DASH NO AND DATE CODE IN APPROX AREA SHOWN

100-04D003-5 5
100-04D003-3 5
100-04D003-1 SHOWN

APPROVED FOR	DATE	APPROVED
PRODUCTION		
PRE-PRODUCTION		
PROTOTYPE		

APPROVALS DATE
H.P.G. 7-77

APPLICATION

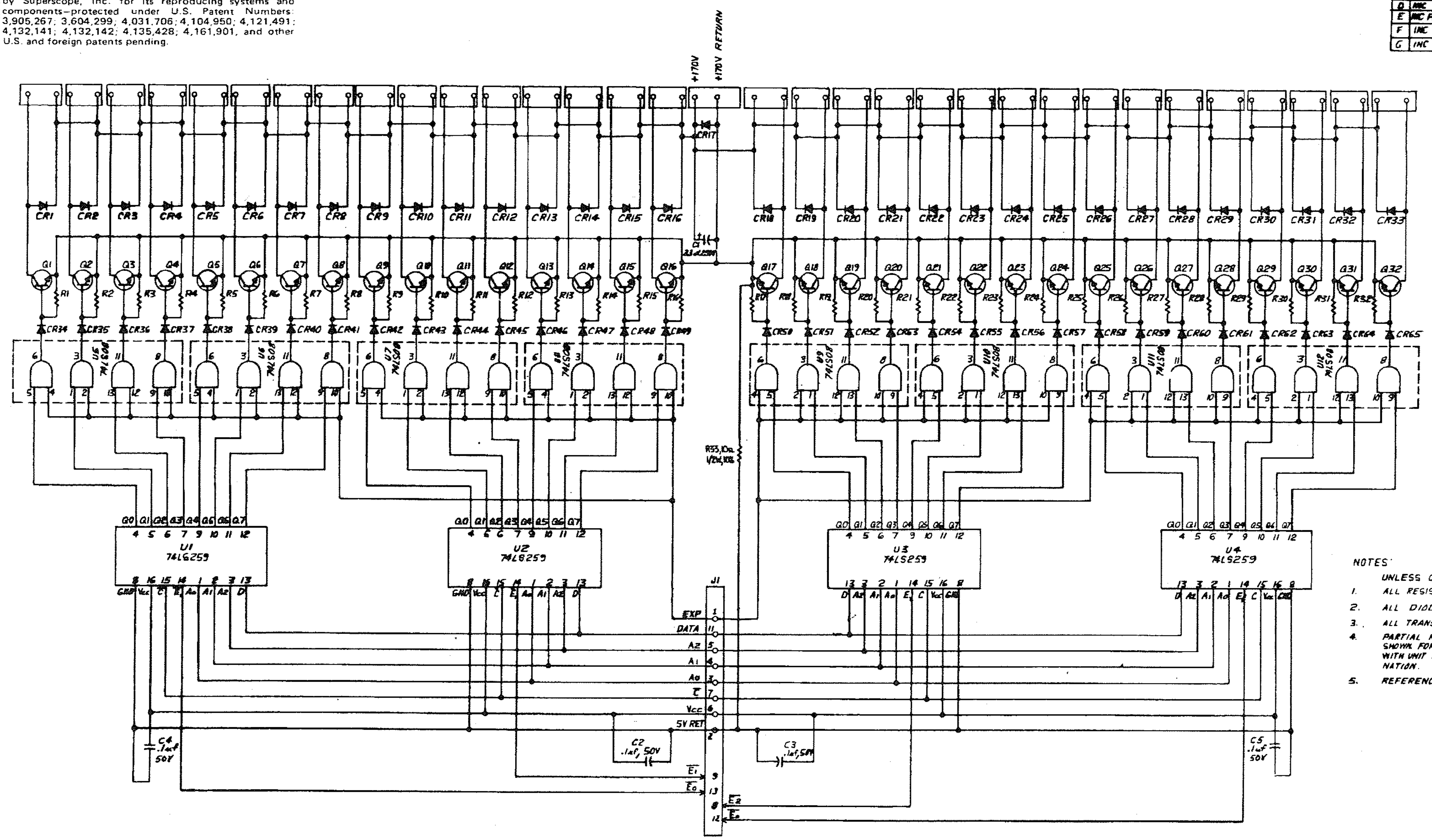
SUPERSCOPE CHATSWORTH, CALIFORNIA

PRINTED WIRING BOARD ASS'Y
DRIVER

D 26687 100-040003 F
2:1

FIGURE 16-B

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	INC PER ECA 5355	10/19/77	
B	INC PER ECA 5384	11/11/77	
C	INC PER ECA 5511	12-28-77	RLS
D	INC PER ECA 5565	1-13-78	
E	INC PER ECA 5672	3-9-78	VRR
F	INC PER ECA 6707	4-3-78	VAR
G	INC PER ECA 5875	7-5-78	



NOTES:

UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE 1K 1/4W, 5%.
2. ALL DIODES ARE 1N4004
3. ALL TRANSISTORS ARE 100-11A002-1
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
5. REFERENCE DRAWINGS:

P.W. BOARD: 100-05D003
P.W. MASTER: 100-08D003
P.W. ASS'Y: 100-04D003
SILKSCREEN 100-07D003

	GND	VCC
U5	7	14
U6	7	14
U7	7	14
U8	7	14
U9	7	14
U10	7	14
U11	7	14
U12	7	14

APPROVED FOR	DATE	APPROVED
PRODUCTION	1-26-78	VB Ramsey
PRE-PRODUCTION	9-12-77	
PROTOTYPE		

QTY REQD	SYM	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION	SPECIFICATION	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS
BREAK SHARP EDGES
MEET DIM. BEFORE/AFTER FINISH
DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMAL .XX ± .XXX ±
ANGLE ±
DO NOT SCALE DRAWING

HOLE DIA	TOLERANCE
.0135 THRU .125	+.004 - .001
.126 THRU .250	+.005 - .001
.251 THRU .500	+.006 - .001
.501 THRU .750	+.008 - .001
.751 THRU 1.000	+.010 - .001
1.001 THRU 2.000	+.012 - .001

MATERIAL
RELEASED
DASH NO.
NEXT ASSY
USED ON
APPLICATION

CONTRACT NO.

APPROVALS	DATE
DRAWN BY STAN NIKESELL	7-18-77
CHECKED	
APPROVAL	
APPROVAL	

DESIGN ACTIVITY APPROVAL
CONTRACTOR APPROVAL

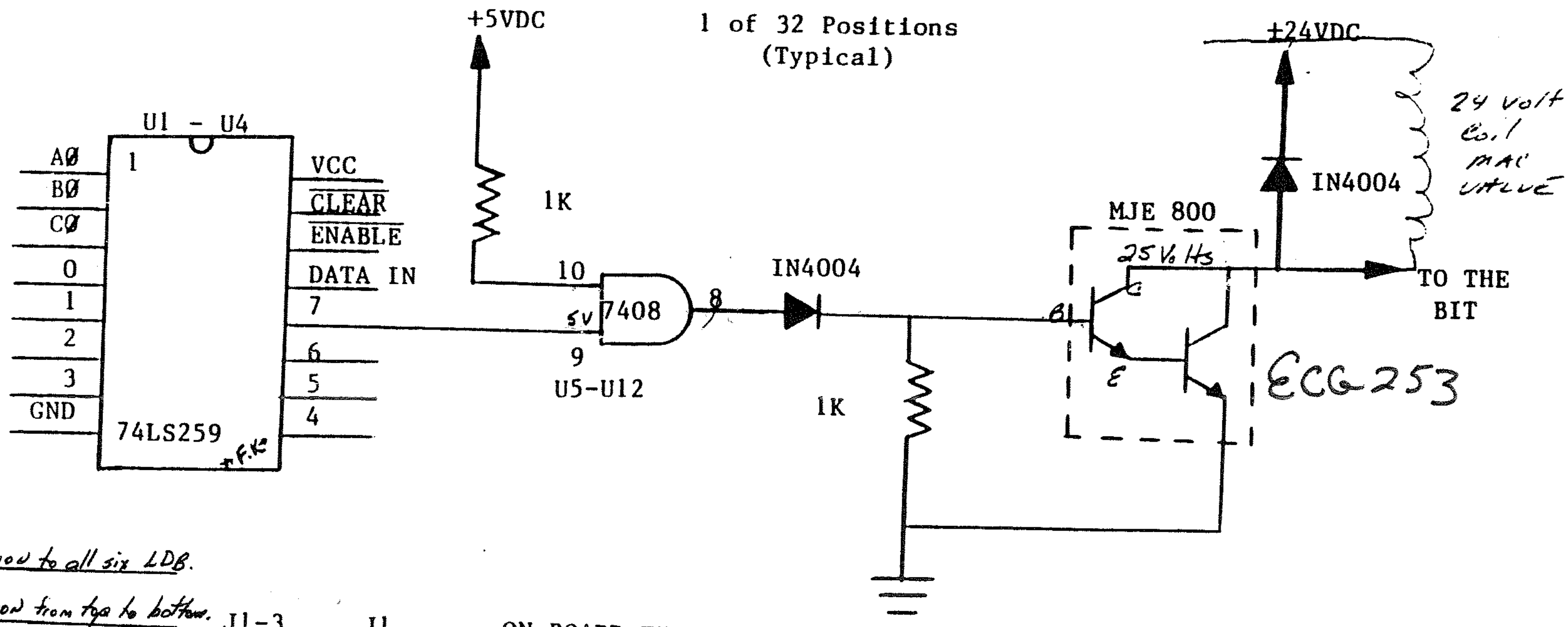
SUPERSCOPE CHATSWORTH, CALIFORNIA

SCHEMATIC
DRIVER

SIZE F
CODE IDENT NO. 26687
DRAWING NO. 100-06F003
REV G
SCALE NONE
SHEET 1 OF 1

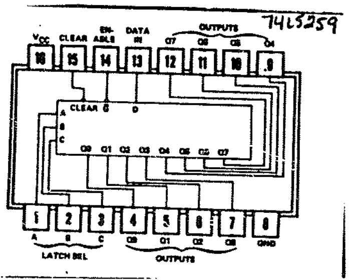
LONG DRIVER BOARD SCHEMATIC (Partial)

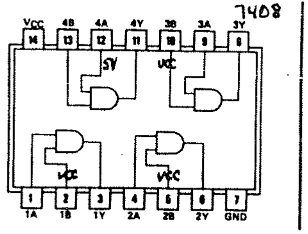
1 of 32 Positions
(Typical)



- *Address lines are common to all six LDB.*
- *ENABLE lines are common from top to bottom.*

J1-3	J1	ON BOARD TIE POINTS
	1	
	2	GND
47	3	PIN 1 U1 - U4
46	4	PIN 2 U1 - U4
45	5	PIN 3 U1 - U4
48	6	VCC (+5VDC)
22	7	PIN 15 U1 - U4
19	8	PIN 14 U3
18	9	PIN 14 U2
	10	KEY
21	11	PIN 13 U1 - U4
20	12	PIN 14 U4
17	13	PIN 14 U1





4 ENABLE LINES PER LDB.

12 ENABLE LINES PER DRAWER

3 Address LINES

2 DATA LINES

74LS259 TRUTH TABLES

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	G			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
* L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H ≡ high level, L ≡ low level
D ≡ the level at the data input
Q_{i0} ≡ the level of Q_i (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.